Notice of Allowability	Application No.	Applicant(s)	
	10/650,325	BAYAN ET AL.	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *papers filed March 1, 2006*.

2. ☒ The allowed claim(s) is/are *1,3,5,6,8,9,11-16,18-23,32,33 and 35-42*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

DETAILED ACTION

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Francis T. Kalinski on May 10, 2006.

Claim 1, (amend)

A substrate panel for use in semiconductor packaging, comprising:

a lead-frame panel, including

an array of device areas, each device area having a die attach pad encircled by & plurality of conductive features, each conductive feature defined by an innermost contact portion, an outermost landing portion, and a connecting lead segment, wherein the innermost contact portion [that] lies proximal to the die attach pad and extends through the [substrate] lead-frame panel to expose a bottom surface on the bottom of the [substrate] lead-frame panel and said conductive feature having the [an] outermost landing portion [having a wirebonding surface] located near an edge of the device area and further away from the die attach pad than the innermost contact portion, the outermost landing portion including a wirebonding surface [near an edge of the device] and having a connecting lead segment that extends between the innermost contact portion and the outermost landing portion wherein the connecting lead

segment is thinner than the innermost contact portion that extends through the [substrate] lead-frame panel; and

a dielectric material that fills spaces between adjacent conductive features and that fills spaces underneath the connecting lead segments, wherein a top surface of the dielectric material is substantially coplanar with the top surface of the [substrate] lead-frame panel and the wire bonding surfaces, and. the bottom surface of the dielectric material is substantially coplanar with the bottom surface of the [substrate] lead-frame panel and said exposed bottom surface of said innermost contact portions, thereby forming [a substrate] lead-frame panel having substantially planar top and bottom surfaces.

Claim 3, (amend)

A substrate panel as recited in claim 1 wherein the outermost landing portions have a portion that is [having the wirebonding surface are] thinner than the [substrate] lead-frame panel, such that the outermost landing portions are not exposed on the bottom surface of the [substrate] lead-frame panel and wherein the dielectric material [of the substrate] is formed underneath thinner portions of the outermost landing portions to give support to the wirebonding surfaces, said support being sufficient to structurally reinforce the wirebonding surfaces during a wire bond process.

Claim 5, (amend)

A substrate panel as recited in claim 1 wherein the device areas are arranged in at least one two dimensional array such that the lead-frame panel [substrate] has at least one two-dimensional array of device areas.

Claim 6, (amend)

A substrate panel as recited in claim 5 wherein the lead-frame panel further comprises a matrix of tie bars, the tie bars being positioned between immediately adjacent device areas in the two dimensional array of device areas and configured to support the device areas [lead-segments].

Claim 8, (amend)

A substrate panel as recited in claim 1 wherein the die attach pad has a plurality of posts exposed on the bottom surface of the [substrate] lead-frame panel.

Claim 9, (amend)

A substrate panel as recited in claim 1 wherein at least one outermost landing portion [wire bonding landing] is directly electrically coupled to the die attach pad by a lead segment.

Claim 11, (amend)

A substrate panel for use in semiconductor packaging, comprising:

a lead-frame panel including a two dimensional array of device areas, each device area having a plurality of conductive features, each conductive feature having,

a contact portion having an exposed bottom surface at the bottom of the substrate panel wherein the contacts are arranged in a microarray configuration,

a landing portion having a wire bonding surface exposed on a top surface of the substrate panel the landing portion is arranged outward from an [the] associated contact portion and thereby closer to an outer edge of the device area than the associated contact portion, and

a connecting lead segment configured to electrically couple each contact portion with its associated landing portion; and

a dielectric material that fills spaces between adjacent conductive features and underlies at least a portion of each of the wire bonding surfaces, wherein a top surface of the dielectric material is substantially coplanar with the top surface of the [substrate] lead-frame panel and the wire bonding surfaces [landings], and wherein a bottom surface of the dielectric material is substantially coplanar with the bottom surface of the [substrate] lead-frame panel and the exposed bottom surface of the contact portion.

Claim 12, (amend)

A substrate panel as recited in claim 11 wherein each device area further includes a die attach pad, the die attach pad being exposed on the top surface of the [substrate] lead-frame panel.

Claim 13, (amend)

A substrate panel as recited in claim 12 wherein the contact portions surround the die attach pad, and wherein the die attach pad has a plurality of posts exposed on the bottom surface of the [substrate] lead-frame panel, the contact portions and the posts being arranged in a two dimensional microarray of rows and columns.

Claim 15, (amend)

A singulated packaged integrated circuit, comprising:

a substrate having an edge, the substrate including a plurality of contacts *configured for* electrical contact underneath the substrate with the contacts having exposed contact surfaces on a bottom surface of the substrate, a plurality of wire bonding landings being located outward from the contacts and more closely to the edge of the substrate and at a top surface of the substrate, lead segments that extend between the contacts and their associated wire bonding landings

electrically coupling the wire bonding landings to associated. contacts, and a first dielectric layer that fills spaces between adjacent lead segments and fills space under the wire bonding landings, wherein a top surface of the dielectric layer is substantially coplanar with the top surface of the substrate and the wire bonding landings, and a bottom surface of the dielectric layer that is substantially coplanar with the bottom surface of the substrate [panel] and substantially coplanar with said contact surfaces, thereby forming [a] the substrate having substantially planar top and bottom surfaces;

a die mounted on the substrate, the die having a plurality of bond pads configured for electrical connection, to the wire bonding landings;

a plurality of connectors for electrically connecting the plurality of bond pads to associated wire bonding landings; and

a second dielectric layer that encapsulates the die and the plurality of connectors and covers at least a portion of the top surface of the substrate.

Claim 20, (amend)

A packaged integrated circuit as recited in claim 15 wherein the substrate further includes a die attach pad surrounded by the [lead] contacts, the die attach pad being exposed on the top surface of the substrate.

Claim 36, (amend)

A substrate panel as recited in claim 1 wherein the plurality of innermost contact portion [contacts] is exposed on a bottom surface of the substrate panel are arranged in a microarray configuration.

Claim 37, (amend)

A substrate panel as recited in claim 36 wherein the plurality of innermost contact portion [contacts] arranged as a microarray are patterned in a ball grid array (BGA) configuration.

Claim 38, (amend)

A substrate panel as recited in claim 8 wherein the plurality of exposed bottom surfaces of the contact portions and the plurality of posts exposed on the bottom surface of the [substrate] lead-frame panel are arranged in a micro array.

Claim 39, (amend)

A substrate panel as recited in claim 38 wherein the exposed bottom surfaces of the contact portions and the plurality of posts exposed contacts and posts on the bottom surface of the [substrate] lead-frame panel are arranged in a BGA pattern.

Claim 40, (amend)

A substrate panel as recited in claim 11 wherein at least one of the landing portions includes a support footing that extends downward from the bottom surface of said landing portions, the footing configured to support the landing portion during a wirebonding process and having an exposed bottom surface that is substantially coplanar with the bottom surface of the [substrate] lead-frame panel.

Claim 41, (amend)

A substrate panel as recited in claim 15 wherein at least one of the wire bonding landings includes a support footing that extends downward from the bottom surface of said wire bonding landings, each footing configured to support the landing during a wirebonding

process and configured to have an exposed surface that is substantially coplanar with the bottom surface of the [substrate] lead-frame panel.

Claim 42, (amend)

A substrate panel as recited in claim 11 wherein at least some of the landing portions are thinner than the [substrate] lead-frame panel, such that the thinner landing portions are not exposed on the bottom surface of the [substrate] lead-frame panel, and at least some of the connecting lead segments are thinner than the [substrate] lead-frame panel such that the thinner lead segments are not exposed on the bottom surface of the [substrate] lead-frame panel.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jmi

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800